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54 **Wafer processing system.**

57 A system for multichamber processing of semiconductor wafers providing flexibility in the nature of processing available in a multiprocessing facility. To accommodate changing processing demands and chamber replacement, a mobile processing chamber selectively docks with a multiple chamber system to form one of its processing chambers. The capabilities of the multiprocessing multichamber system are enhanced by extending the system to other multichamber systems through intermediate buffer storage wafer cassette and elevator systems. The extended multichamber system is further provided with intermediate access wafer storage elevator cassettes.

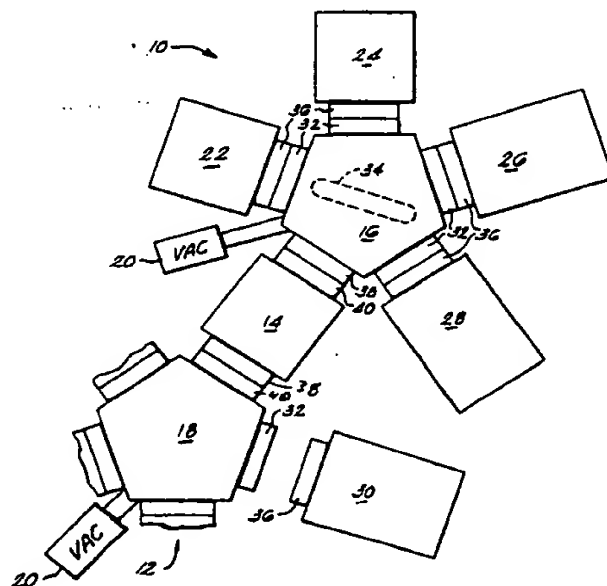


FIG. 1

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WAFER PROCESSING SYSTEM

The present invention relates to the processing of semiconductor wafers in plural chambers. As shown in our commonly assigned U.S. Patent No. 4,715,921, issued December 29, 1987 and U.S. Patent Applications Serial No. 853,775, filed April 18, 1986, and Serial No. 115,774, filed October 30, 1987, the use of plural chambers to process semiconductor wafers permits more efficient, rapid and flexible semiconductor wafer plasma environment processing. In that disclosure the ability is provided to address the wafers in an individual cassette to different ones or multiples of processing chambers associated with that one cassette.

In the use of multiple chambers it can occur that one or more chambers must be serviced. Time is lost in the process of repairing or converting those chambers to other functions due to the extended period of time needed to bring chambers to the vacuum state needed to process semiconductor wafers.

According to the teaching of the present invention a multi processing, multichamber system is provided in which processing chambers associated with a multichamber multiprocessing facility are readily exchangeable to minimize "down time" and in which the use of buffer wafer storage elevator cassette systems is utilized to expand the number of processing chambers and provide wafer input and output access at intermediate points.

According to one embodiment of the invention, a cluster of processing chambers are arrayed about a wafer transport. One or more of the processing chambers is provided as a mobile system which may be selectively attached and detached to the wafer transport system without loss of the controlled environment within the transport and other chambers and without loss of the controlled environment within the mobile processing chamber itself. Each mobile chamber is equipped with its own evacuation capability along with the electronics for generating plasma, sputtering or other processing conditions within the processing chamber and with a gas feed system for supplying appropriate environmental gases to the chamber. The mobile character of the chamber permits the multichamber facility to continue to operate without complete breakdown in the case where it is desired to exchange one chamber for a chamber of a different processing type or to repair a chamber. Additionally, by providing back-up chambers in a pre-evacuated condition ready for selective attaching to a multichamber facility, the long down time necessary to pump down the system is avoided by keeping the remainder of the processing system at the environmentally controlled, typically low pres-

sure environment, while the selectively attachable pre-evacuated chambers are attached and decoupled at the appropriate controlled environment. This necessitates the evacuation of only a small portion of unwanted gases which typically enter the system or mobile chamber through the docking mechanism that provides selective attachment of the mobile chamber to the multichamber multiprocessing facility.

In another embodiment of the invention the flexibility of multichamber multiprocessing facility is enhanced by coupling plural such facilities through intermediate wafer buffer storage cassette and elevator systems. Additionally, a wafer transport path, contained within a closed environment, is provided between elevators with an access elevator system along the transport path to permit intermediate wafer input and output.

These and other features of the present invention are more fully described below in the solely exemplary detailed description and accompanying drawing of which:

Fig. 1 is an overhead view of a multichamber multiprocessing system having plural multichamber facilities and mobile processing chambers with a wafer buffer storage cassette and elevator system between multichamber facilities;

Fig. 2 is an elevational partially interior partially sectional view of a docked mobile chamber for use in the embodiment of Fig. 1;

Fig. 3 is an illustration of a wafer transport system for transporting wafers between buffer storage cassette elevator systems and providing access along the transport path for wafer insertion and removal; and

Fig. 4 is a view of the transport mechanism within a controlled environment enclosure of Fig. 3.

The present invention contemplates a system for providing multichamber multiprocessing of semi-conductor wafers in which individual processing chambers are mobile to permit easy exchange of processing chambers without requiring the down time for complete system evacuation and further for permitting flexible extension of processing capabilities by joining multi-processing multichamber facilities through a wafer buffer storage cassette and elevator system that may include intermediate buffer storage that permits wafer insertion and removal from the overall processing system.

Such a system is illustrated in Fig. 1 in which a multichamber multiprocessing facility 10 is connected to a second such multichamber multiprocessing facility 12 through an intermediate cassette system 14 which typically comprises a multi wafer containing cassette and elevator for position-

ing each wafer slot in the cassette at a point where it can be accessed by a transfer arm contained within respective transfer mechanisms 16 and 18 of the multiprocessing facilities 10 and 12. Each transport mechanism 16 and 18 is typically provided with a vacuum pump 20 capable of evacuating at least the interior of the transport mechanism 16.

Arrayed about each transport mechanism 16 are a plurality of multiprocessing chambers. Those arrayed about the transfer mechanism 16 are illustrative of a typical single multiprocessing facility. As shown there processing modules 22 and 24 are of a type which may be permanently associated with the transfer mechanism 16 while processing modules 26 and 28 are mobile processing modules, more fully illustrated below in Fig. 2.

Each of the chambers 22, 24, 26 or 28 are coupled to the transport mechanism 16 through a valved access port and docking mechanism comprising first parts 32 containing a slit access valve, as more fully illustrated in Fig. 2, through which a semiconductor wafer may be passed from the transport mechanism 16 on an arm 34 into and out of the respective chambers 22, 24, 26, 28 (or mobile chamber 30 for mechanism 8) through a further valve and docking mechanism 36 associated with each of the chambers 22, 24, 26, 28 (and/or 30 for mechanism 18). The cassette elevator 14 is similarly coupled through a valve and docking mechanism 38 of the same type associated with the transport mechanism 16 and spacer collars 40 associated with the cassette elevator 14. Because the cassette elevator 14 does not contain a gaseous wafer processing environment it is normally unnecessary that the spacer 40 have a valve associated with it, but a spacer 40 is provided so that the distance between wafers in the cassette 14 and the pivot point of arm 34 can be made the same as the distance between that pivot point and the point at which wafers are placed within each of the processing chambers 22, 24, 26, 28, and 30.

Reference is additionally made to United States Patent No. 4,715,921, issued December 29, 1987 and U.S. Patent Applications Serial No. 853,775, filed April 18, 1986 and Serial No. 115,774, filed October 30, 1987 in which portions of the structure of the Fig. 1 apparatus are additionally illustrated. The details of mobile processing chambers 26, 28 and 30 are illustrated more fully below with respect to Fig. 2.

As shown in Fig. 2 each of the chambers 26, 28 and 30 includes a housing 50 in which a module 52 is installed and that contains a chamber 54, having a pedestal 56 supporting a cathode 58 on which a wafer 60 is typically placed below an anode 62 from which, in the example of plasma processing, an electric field emanates to produce a

plasma discharge for processing of the wafer 60. The module 52 additionally includes electronics 64 which in the case of plasma discharge provides the appropriate field between the anode 62 and cathode 58 as known in the art. The module 52 may also contain an environmental gas control system 66 to supply appropriate etching gases in the case of plasma etching or gases for other purposes as described below. The control of the electronics and environmental gas supplies 64 and 66 is under the direction of a micro-processor 68 located within the housing 50.

The module 52, in the specific illustration of Fig. 2, is intended for plasma etching of the surface of the wafer 60. Other modules can be provided that will employ other processing technologies such as chemical vapor deposition, sputtering, rapid thermal processing, rapid thermal annealing, plasma cleaning to name a few, and utilizing technology and apparatus already known in the art.

The module 52, as installed within the housing 50, mates, for wafer exchange and transfer, with the wafer transfer mechanism 18 through coupling and docking valves 32 and 36. In particular each such valve includes a conduit 70 and 72 which are fastened to the mechanism 18 and module 52 respectively. The conduits 70 and 72 have outer beveled flanges 74 and 76 respectively which are joined through a quick connect band 78 typically hinged at a hinge 80 and coupled with a clamp 82. Locating pins 84 are typically provided to accurately align the conduits 70 and 72 and thus module 52 with respect to the transfer mechanism 18 so that a wafer may be inserted through the conduit 70 and 72 into the chamber 54 and onto the cathode 58.

To facilitate this alignment, the housing 50 rolls upon a dolly system 86 which is adjustably supported from the base of the housing 50 through adjustment screws 88. Conduits 70 and 72 are typically elongated in the dimension in out of the page in order to accommodate the full width of a semiconductor wafer.

In order to seal the controlled environment within the transfer mechanism 18 and within the chamber 54, valve assemblies 90 and 92 are provided within the conduits 70 and 72 respectively to seal access ports 91 and 93 into the respective interiors. Valves of this type are illustrated in the above-identified, commonly assigned patent and applications.

Seals 94 may be additionally provided in the facing surfaces of the conduits 70 and 72.

The interior of the chamber 54 is connected through a manifold 100 through a series of conduits 102, 104, 106 and computer controlled valve 108 to a turbo pump 110 which is in turn conducted through an output conduit 112 to an exhaust mani-

fold 114, computer controlled exhaust valve 116 into an exhaust pipe 118 which exits through the housing 50 for attachment to a further exhaust and vacuum pump and to processing equipment for exhaust gases.

A conduit 120 feeds directly off the conduit 102 into the manifold 114 and then through the controlled valve 116 to the outlet 118.

In operation the computer 68 controls the turbo pump 110 and its power supply 122 in conjunction with the valves 108 and 116 and additional vacuum pump systems external of the housing 50 to provide rough and final exhausting of the chamber 54. Vacuum pump 20 evacuates the conduits 70 and 72 after docking.

Fig. 3 illustrates a further embodiment of the invention wherein a pair of cassette elevators 140 and 142 are coupled to a respective pair of transfer mechanisms 144 and 146 through associated valve interfaces 148 and 150, corresponding to the mechanisms 32 and 36 shown above. Wafers are transferred through a conduit 152 between the elevator systems 140 and 142. Intermediate along the transfer conduit 152 is an elevator cassette 154 providing access to the conduit 150 for the insertion and removal of wafers to be processed or after processing.

The actual transfer mechanism within the conduit 152 is illustrated in greater detail in Fig. 4. As shown there a linear guide 160 has a slide 162 driven along it by a drive mechanism 164. On top of slide 162 is an arm 166 and a further slide 168 running thereon, under positional control of the drive mechanism 164. The slide 168 contains a wafer arm 170 which can be extended into the cassette of elevators 140, 142, and 154 for the retrieval or insertion of a semiconductor wafer. The arm 166 is positioned either parallel to the guide 160, facing in either direction, or perpendicularly disposed into the elevator cassette 154 when in a central housing 172 positioned along the conduit 152. The position of the guide arm 166 is controlled by a rotatable hand 174 which can be elevated and dropped to engage the arm 166 at a central point 176 under the control of a drive and elevation mechanism 178 (Fig. 3) either automatically under computer control or by manual manipulation.

In this manner cassettes can be applied to the multichamber multiprocessing system associated with either of the transfer mechanisms 144 and 146 by loading into the corresponding cassette elevator systems 140 and 146 through the conduit 152 from the elevator 154. In this manner wafers can be exchanged between the elevators 140, 142 and 154 in any desired sequenced to accomplish a broad range of wafer processing activities within the respective multiprocessing systems associated with

each transfer mechanism 144 and 146. A plurality of additional intermediate elevator cassettes 150 of the type of 154 may be applied along the conduit path or the path of conduit 152 in order to include as many multi-processing facilities as is desired.

Claims

1. A portable semiconductor processing chamber assembly characterized by a mobile housing including means for permitting movement of said housing over a surface, a chamber supported by said housing for controlled environment processing of a semiconductor wafer, means associated with said housing for establishing a controlled environment within said chamber, means for docking said chamber with a semiconductor wafer transfer mechanism to permit transfer of a semiconductor wafer between said transfer mechanism and said chamber through a confined environment.

2. A portable semiconductor processing chamber assembly according to claim 1, characterized in that the housing includes means for adjusting the height and attitude of said housing to permit accurate docking.

3. A portable semiconductor processing chamber assembly according to claim 1, characterized in that the means for establishing a controlled environment within said chamber includes means supported with said housing to provide gas evacuation of said chamber.

4. A portable semiconductor processing chamber assembly according to claim 3, characterized in that the gas evacuation providing means includes means for coupling to a further evacuation means.

5. A portable semiconductor processing chamber assembly according to claim 1, characterized in that said docking means includes a conduit and means for mating said conduit with a complimentary conduit on said transfer mechanism, and in that quick connect/disconnect means are provided between said conduit and complimentary conduit.

6. A semiconductor wafer multiprocessing system, characterized by a transfer station, means for storing semiconductor wafers, and a plurality of semiconductor processing chambers associated with said transfer station to permit transfer of semiconductor wafers between said storage means and said processing chambers.

7. A semiconductor wafer multiprocessing system characterized by means for storing semiconductor wafers, a first transfer station, a first plurality of semiconductor processing chambers associated with said first transfer station to permit transfer of semiconductor wafers between said storage means and said first plurality of processing chambers, a

second transfer station, and a second plurality of semiconductor processing chambers associated with said second transfer station to permit transfer of semiconductor wafers between said storage means and said second plurality of processing chambers. 5

8. A semiconductor wafer multiprocessing system characterized by first, second and third means for storing semiconductor wafers, a first transfer station, a transfer mechanism for transferring semiconductor wafers between said first and third and said second and third storing means respectively, a first plurality of semiconductor processing chambers associated with said first transfer station to permit transfer of semiconductor wafers between said storage means and said first plurality of processing chambers, a second transfer station, and a second plurality of semiconductor processing chambers associated with said second transfer station to permit transfer of semiconductor wafers between said storage means and said second plurality of processing chambers. 10 15 20

9. A semiconductor wafer multiprocessing system according to claim 8, characterized in that the transfer mechanism includes an arm, a track, means for guiding said arm along said track between said first and second storing means passed said third storing means, and means for extending said arm from said track into said first, second and third storing means. 25 30

10. A semiconductor wafer multiprocessing system according to claim 9, characterized in that means are provided for changing a direction of said arm between pointing along said track toward said first or second storing means and away from said track toward said third storing means. 35 40 45 50 55

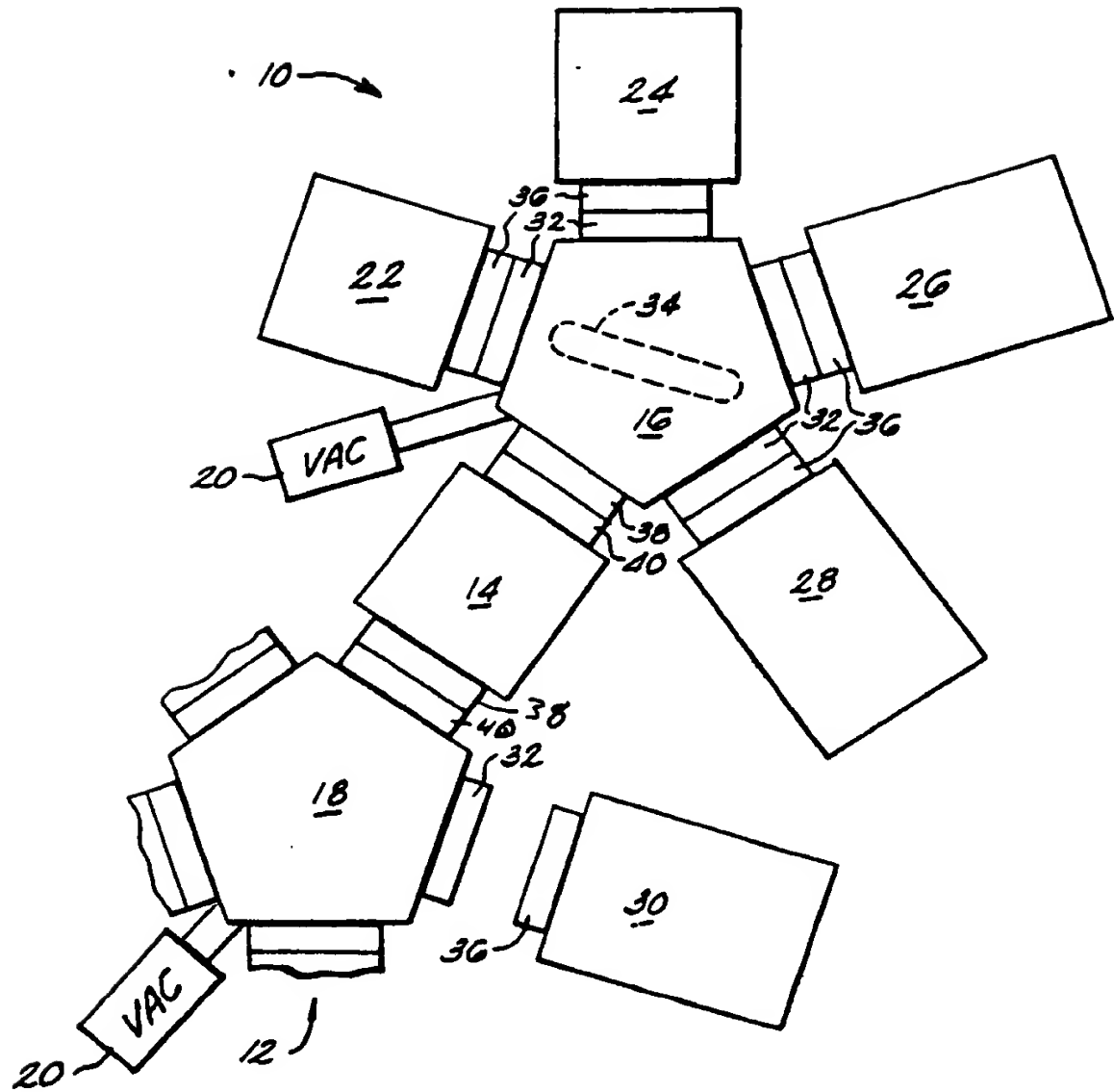


FIG. 1

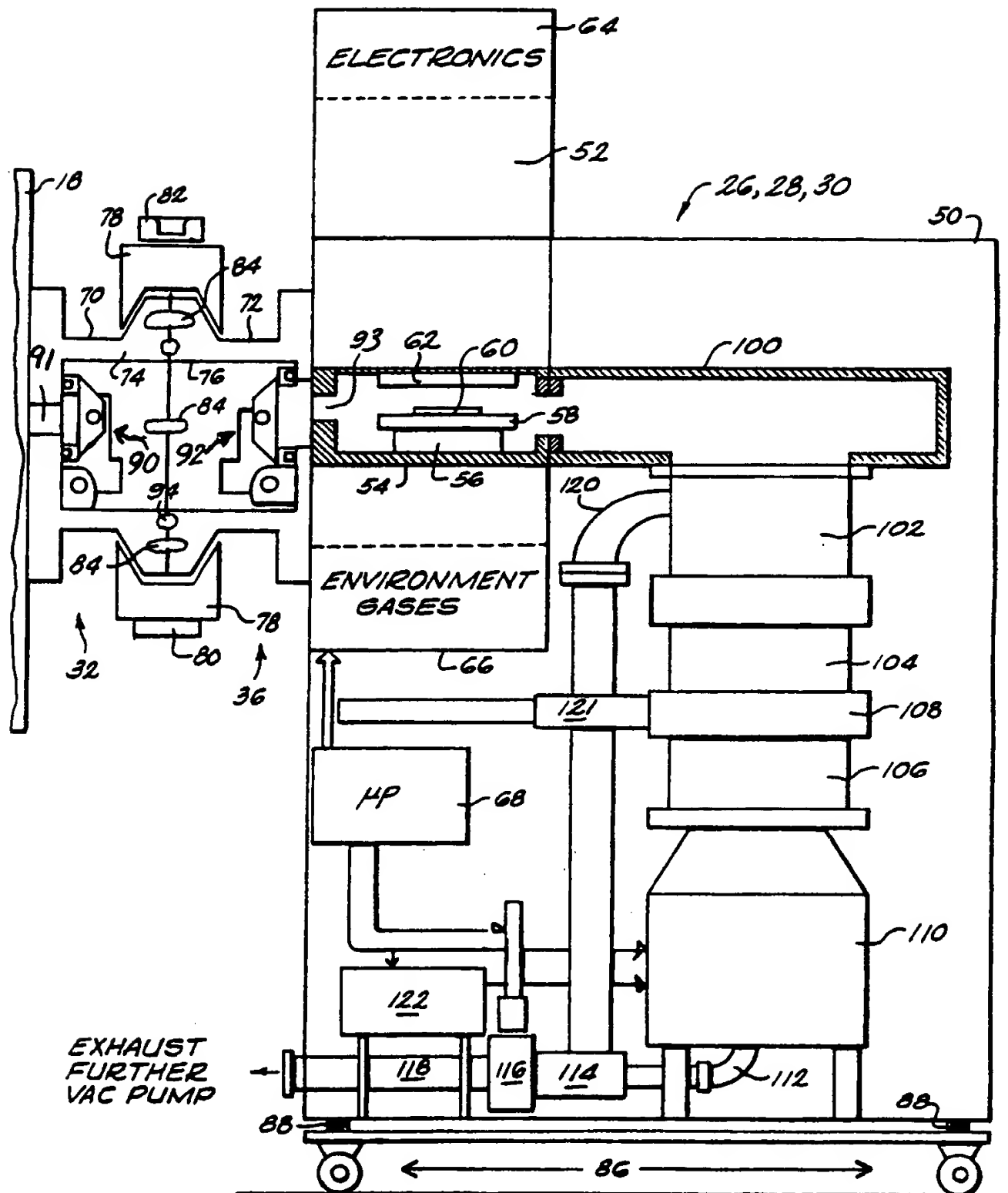
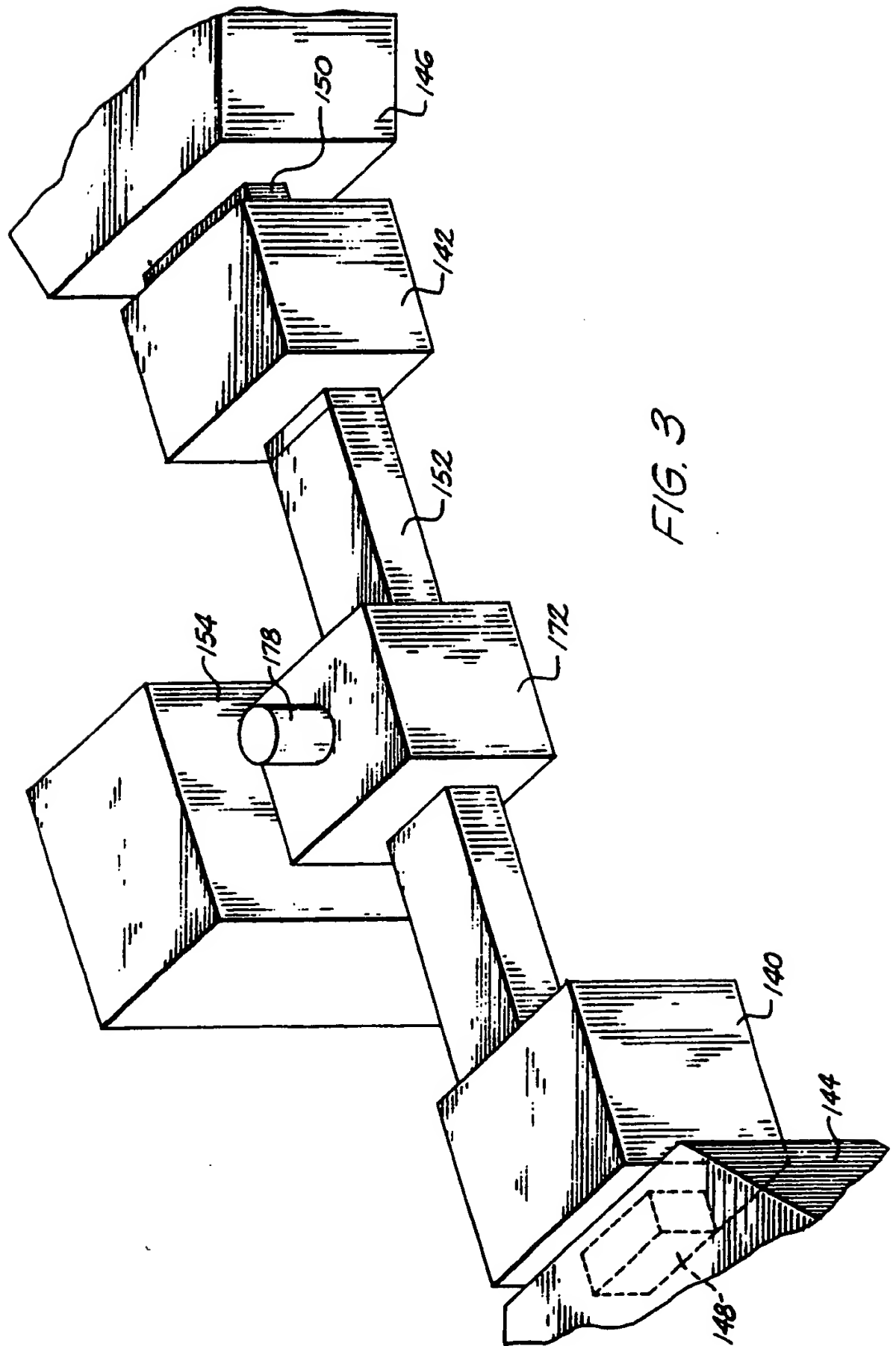


FIG. 2



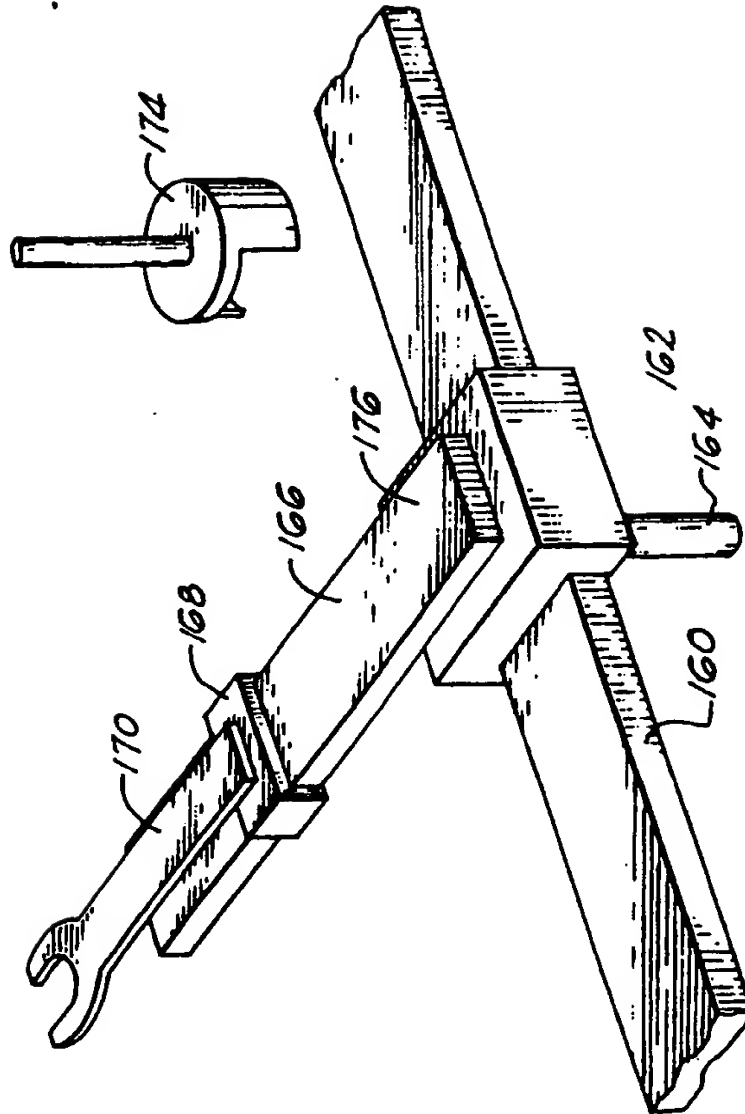


FIG. 4

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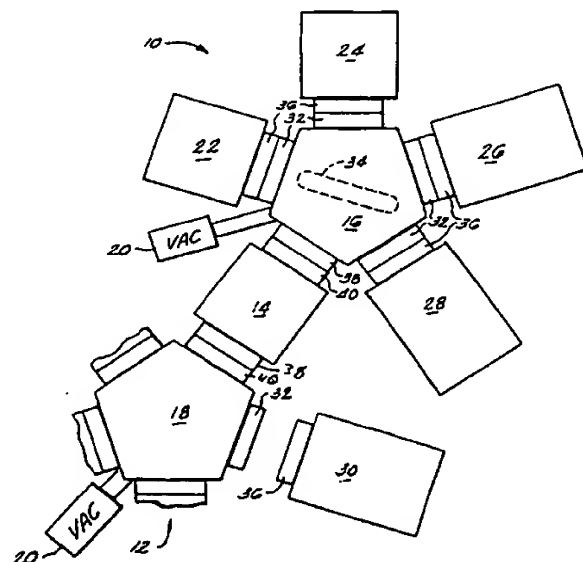
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W-8000 München 2(DE)(54) **Wafer processing system.**

(57) A system for multichamber processing of semiconductor wafers providing flexibility in the nature of processing available in a multiprocessing facility. To accommodate changing processing demands and chamber replacement, a mobile processing chamber selectively docks with a multiple chamber system to form one of its processing chambers. The capabilities of the multiprocessing multichamber system are enhanced by extending the system to other multichamber systems through intermediate buffer storage wafer cassette and elevator systems. The extended multichamber system is further provided with intermediate access wafer storage elevator cassettes.

**FIG. 1****EP 0 377 464 A3**



European
Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 90 10 0164

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP-A-0 272 141 (APPLIED MATERIALS) * column 15, line 4 - column 16, line 4; figure 20 *	1	H 01 L 21/00
A	US-A-4 657 618 (SPENCER) * column 3, line 58 - column 4, line 59 *	1	
D,A	US-A-4 715 921 (MAHER)		
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			H 01 L
The present search report has been drawn up for all claims			
Place of search		Date of completion of search	Examiner
The Hague		13 May 91	BERTIN M.H.J.
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